XDP Electronics Whitepaper
Analysis of Acquisition Architectures

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Introduction

The electronics for a flow cytometer serve a critical role in data acquisition. Analysis and ultimately sort decisions can only be as good as the input data, so acquisition is responsible for providing high quality data. This becomes challenging, as the input data can contain DC content from millivolts to volts that needs to be removed, can easily stretch across four or more decades of dynamic range, can contain populations with very little separation and can occur with narrow pulses as brief as 400 ns at event rates exceeding 100,000 events per second. Additionally, the need for post processing for compensation and to generate other computed parameters drive, a need for very linear data with high resolution.

Different architectures have been developed over time to address the needs of acquisition. This paper attempts to examine and compare some of the more common architectures that have been deployed in the field. Only architectures utilized on sorters are examined at this time.

Acquisition Architecture Descriptions

Analog Track and Hold

Description

One of the first prolific acquisition architectures, the Analog Track and Hold (T/H) architecture is still in use today on some instruments. This architecture uses an analog approach for peak determination of the linear, logarithmic and integral values during a gated window and then digitizes the peak values at the end of the window.[1] An example of this type of system is shown in Figure 1.

This architecture uses an analog Baseline Restoration unit to approximate and remove DC offsets, an Integrator to calculate the area of the input during an event, a Log Amp to calculate the logarithm of the input data to view high dynamic range, a Mux to select which input should be sampled, a Track and Hold circuit to measure the maximum amplitude during the defined event and finally an Analog to Digital Converter (ADC) to convert the maximum value at the end of the event to digital. A timing and control circuit, not shown, controls the mux and all timing, including clearing the integrator, opening, closing and clearing the Track and Hold circuit and the ADC conversion signals. Additionally, for multiple laser paths to be used, timing signals are used to delay the control signals from the event start for any subsequent laser path.

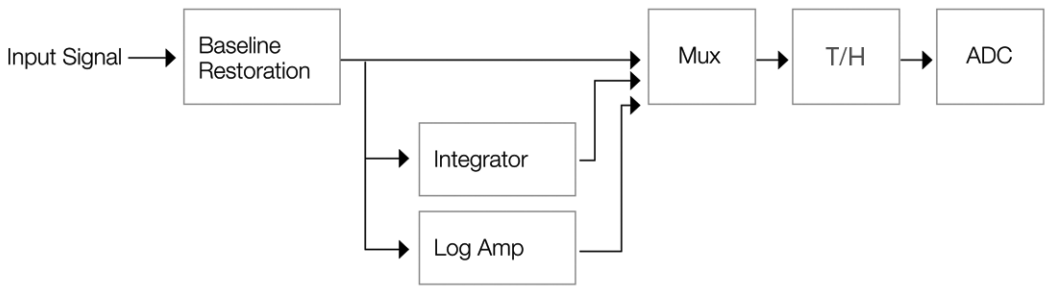

Figure 1 – Analog Track and Hold Block Diagram

Variations on this basic architecture are possible. One possible variation includes having a Track and Hold circuit for each data type and a mux afterwards to digitize each data type to increase parameters per detector.

The pre-XDP MoFlo™ utilizes the basic Track and Hold architecture described above. The Cytopeia inFlux® once utilized the basic Track and Hold architecture and, as of ISAC 2006 was still using some form of Track and Hold (Cytopeia, personal communication). However, more recent information may indicate that they are using a variation to allow collection of more data, or are or will be changing architectures entirely.

Strengths

The primary strength of the Track and Hold architecture is the relative simplicity of building one to achieve basic sampling of event data without needing much digital processing. Thus, with basic building blocks available many years ago, this was one of the only architectures that could feasibly be utilized.

With simple digital requirements, this architecture can operate at high event rates without requiring tremendous amounts of backend processing. Simple digital requirements also mean that processing does not depend on pulse width, so narrow pulses can be captured.

Another advantage is that it allows selection of multiple parameters, giving the instrument software or operator choices for how to analyze the data.

Use of a log amp also achieves a higher dynamic range than using an ADC alone can achieve, giving this architecture an advantage for the dynamic range of the data.

A summary of strengths:

- Simple architecture
- High Event Rates
- Capable of processing narrow pulses
- Choice of multiple parameters
- Log amp provides high dynamic range

Weaknesses

This architecture does, however, contain a number of weaknesses. First, this architecture relies on analog gates being opened during specific times and then being held until conversion at the end of the event. This introduces two problems: you cannot collect data from a previous laser if a later laser is used for triggering as the data has already been missed and there is a dead time at the end of the event during mux settling, ADC conversion and then T/H discharge where input data cannot be examined. This reduces triggering options and creates dead spots where new events cannot be examined or are only partially examined.

Second, in the basic architecture, only a single parameter can be measured for each detector. This reduces the amount of data collected and the options with which to discriminate cells or particles from each other.

The Baseline Restoration also relies upon analog methods only, which can approximate the true DC offset but are still prone to error at very high event rates. This is because an analog BLR typically gains the input signal, clamps during pulses, integrates and feeds the integral back as an offset to sum into the input. Thus, during normal slow operation, any offset error will continually be integrated and fed back, forming a self-nulling loop. However, clamping the pulses works fairly well at slower event rates, but at high event rates the time during pulses becomes greater than the time at baseline and even the clamped pulses start to appear as a positive offset. This integrates into a positive value and causes a negative offset to appear with the data. Even a small drift can cause a proportionally large change to dim events that have small amplitudes themselves.

Another problem with this architecture is that log amps themselves have errors associated with the transfer curve from linear to log. These errors generally come from the log amp internal construction, which is typically a successive compression technique, involving multiple stages. The stages do not perfectly match up, resulting in a non-linear output. This can result in compensated data that does not perfectly center around zero on the axis, but drifts away at certain points. Log amps also compress the upper decade, resulting in lower resolution for compensation to utilize.

Also, by not sampling digitally, there is no possibility of extracting additional parameters.

A summary of weaknesses:

- Triggering only possible from first laser without loss of data
- Dead time between events
- Limited parameters per detector
- Baseline Restoration errors at high speeds
- Log Amp non-linear behavior and lower resolution upper decade
- Single digitization event prevents pulse processing

Analog/Digital Hybrid

Description

In an attempt to create a system with high dynamic range that could eliminate the log amp, the Analog/Digital Hybrid architecture was designed. This system uses Track and Hold circuitry similar to the Analog T/H method, but utilizes multiple gain stages to eliminate the log amp.[1, 2] An example is shown in Figure 2.

This architecture uses an analog Baseline Restoration circuit to approximate and remove DC offsets, three paths for parameter measurement, a mux to select which parameter should be digitized and finally an ADC for digital conversion. The paths for parameter measurement each consist of a type detector to measure peak, integral, or pulse width, followed by a Track and Hold amplifier. A mux circuit selects either the output of the Track and Hold circuit or the output of a precision amplifier that is 32 times the output of the Track and Hold. The output of the mux is captured by a second Track and Hold circuit. The 32X gain stages are used to amplify small signals to get higher resolution measurement from the ADC. To measure small signals, the high gain stage is used and for large signals the direct path is used. The comparator and mux circuit determines which value to measure and also dithers between the two in the transfer region to smooth any gain and offset differences. The two Track and Hold circuits

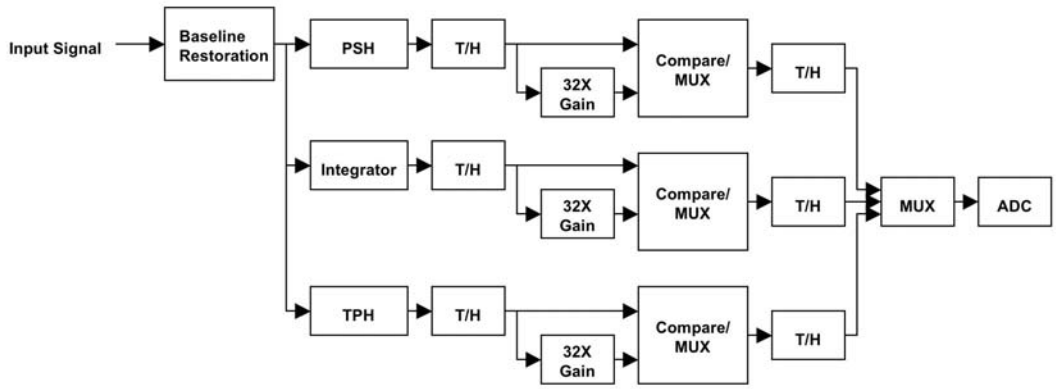

Figure 2 – Analog/Digital Hybrid Block Diagram

are used to allow conversion of one event while another event is being collected by the analog front end to decrease dead time by removing the conversion time from the total dead time.

This architectural approach is used by Beckman Coulter on their newer instruments.[1]

Strengths

The primary strength of this architecture is achieving high dynamic range with less linearity error than a log amp. The gain of 32 stage effectively adds 5 bits to the theoretical conversion resolution for small events, adding a little over a decade. This system can then achieve an objective of four decades of dynamic range while still providing high resolution data for large signals to help compensation algorithms.

A second strength is that the peak, integral and pulse width can be acquired simultaneously from a detector, providing more information and options to the sort logic and operator.

Utilizing additional Track and Hold circuits allows dead time to be reduced by eliminating the ADC conversion from the dead time requirements.

The 32X gain amplifiers are sandwiched between two Track and Hold amplifiers which decreases its bandwidth requirements. The 32X gain is set by the ratio of two resistors that are in the same package to control thermal effects.

With simple digital requirements, this architecture can operate at high event rates without needing tremendous amounts of backend processing. Simple digital requirements also mean that processing does not depend on pulse width, so narrow pulses can be captured.

A summary of strengths:

- High dynamic range
- Linearity improved over log amps help compensation accuracy
- High resolution for small and large peaks helps compensation
- Multiple parameters measured per event
- Reduced dead time
- High event rates
- Capable of processing narrow pulses

Weaknesses

Weaknesses in the Hybrid Analog/Digital architecture stem from the analog processing of events. First, this design relies upon Track and Hold circuits as does a basic Analog T/H architecture and thus only the first laser can be used for triggering without losing data.

Second, while dead time is reduced, there is still time required for mux settling and then Track and Hold discharge preventing a full zero dead time approach.

An analog BLR is still used, which can introduce errors at high event rates.

Considerable circuitry is required to implement the three channels for each detector and multiple gain stages and Track and Hold circuits.

Also, by not sampling digitally, there is no possibility of extracting additional parameters.

A summary of weaknesses:
- Triggering only possible from first laser without loss of data
- Dead time between events
- Baseline restoration errors at high speeds
- Considerable circuitry requirements
- Single digitization event prevents pulse processing

"Digital" Processing with Single ADC Measurement

Description

In an attempt to alleviate some of the problems with Analog T/H circuits and log amps, a new architecture was created that removed both of these circuits and replaced them with a high speed ADC.[1] This type of system is often called "Digital" or "Fully Digital" or "100% Digital". The naming of this system and the comparison to other systems have been quite muddled for some time as sales representatives and marketing from some companies have pushed the "Fully" and "100%" labels. In reality, all conventional flow systems start with an analog signal from a PMT or photo detector and end up as digital data after analog to digital conversion. Thus, no system is "Fully" digital and even the "Analog" systems are not purely analog. However, the "Digital" system is generally used to indicate that there are no log amps or Track and Hold circuits used and that the data is measured with a single ADC. An example of one of these architectures is shown in Figure 3.

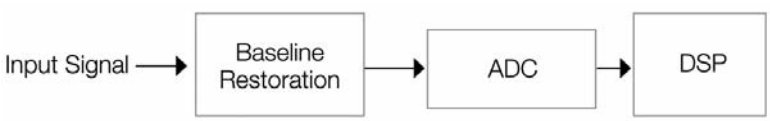

Figure 3 – Digital Processing Block Diagram

This architecture uses an analog Baseline Restoration circuit to approximate and remove DC offsets, a high speed Analog to Digital Converter to digitize the input data and a Digital Signal Processor to perform measurement extraction. Typically, the DSP does a frame based processing where it examines data in chunks, either to find and correlate events or to process a frame of data as it pertains to only the specific event data. The latter reduces the amount of data for the DSP to input, but requires other processing first to isolate, store and transfer just the event data to the DSP. Mathematical processing is utilized to extract parameters such as height, integral, pulse width or others. Computational filtering is also generally used to attempt to increase dynamic range and further computation is used to convert the linear data into a log value for display. Either multi-board control signals or bus communication is used to synchronize multiple board or channels and because the data is stored digitally a simple offset in memory can be used to account for laser delays.

A permutation on this system uses a digital BLR, or a combination of analog and digital BLR or offset control to remove the DC component. By digitally sampling the input data, better algorithms can be used to determine the true DC value and baseline errors can be reduced at higher event rates.

Currently, this architecture is used by the FACSDiVa® electronics on systems from BD Biosciences.[1] Claims have been heard from sales representatives about having digital baseline correction, but hardware evidence to this point has indicated it would account for fine offset control only. However, depending upon how this is done they still may be able to reap most of the benefits of digital baseline restoration.

Strengths

The primary strength of the Digital architecture is the simplicity of the hardware. Very little is required to make this work and it is therefore easy and cheap to build. This benefit is diluted somewhat by the more complicated digital control and processing needed, but this is not overly difficult.

By eliminating the Analog T/H and acquiring data continuously, any laser can be triggered off of without losing data by simply adding memory offsets. This increases triggering options.

Digital techniques can be used to process one event while acquiring another virtually to eliminate dead time. Flexible window extensions can also be used to add options to the time during which pulses are processed, adding margin for fluidic or laser shifts.

Multiple parameters can be extracted from the input signal without adding hardware, giving more options to the sort logic and operator.

Digital or hybrid BLRs can be used to help reduce errors at high event rates.

By not using a log amp the linearity can be improved, providing more accurate data. The upper decade is also not compressed which provides higher resolution data in this area for compensation.

A summary of strengths:

- Simple hardware
- Increased triggering options by not losing previous data
- Little dead time and more flexible windowing
- Pulse processing allows flexible parameter extraction
- Digital or hybrid BLRs for reduced errors
- Improved linearity and higher resolution top end data

Weaknesses

The benefits of the Digital Processing with Single ADC architecture come at the expense of a considerable weakness in limited dynamic range. The best ADCs currently available are 16-bit converters with a signal to noise ratio of around 78dB. This sounds good, but there are a couple of problems. The first problem is low end resolution; the converter may say 16-bits, but some bits are nothing but noise and the real number of bits is somewhat less. With lower frequency content such as for pulse events in flow cytometry, the Effective Number of Bits is calculated by:[3]

ENOB = (SNR – 1.76) / 6.02

This yields a result of 12.66bits for an SNR of 78dB, which, when converted to bins by 2^ENOB, yields 6472. This approximates the actual performance of the converter's ability to digitize the input signal into a final value. With only 6472 discrete values to convert to accurately, a table of output value vs. input voltage over a 4 decade dynamic range is:

Voltage:	Bin:
10V	6472
1V	647
0.1V	64
0.01V	6
0.001V	0

The first problem apparent here is that the bottom decade only has 6 total bins, providing very low resolution. This is often called "picket fence" behavior and has the disadvantage of making those particular bins have a lot of values fall into them and giving them artificial height in a histogram. The second problem is that because a full decade of bins does not exist for the bottom decade, it indicates the noise is greater than the minimum input and the input at this level will thus be completely dominated by noise.

Complicating this problem is the fact that SNR is calculated with the RMS of the noise, but in flow cytometry peak detection is important. For ADC converter noise, which is approximately Gaussian, the peak noise is about 6.6 times[3] the RMS noise. In our example above, with an SNR of 78dB, the RMS noise would be ~0.8 counts for a peak noise of ~5.4 counts, or nearly the full amplitude of the fourth decade! This will dwarf the actual value of the input and make close populations indistinguishable.

Digital filtering is used to help smooth some of this noise, but there is still a significant loss of dynamic range compared to a log amp. Using an area calculation which tends to integrate out some of the noise can also help, but it is still difficult to expand the dynamic range, as the final output data can only get so much better than the input data. However, this is one reason that companies such as BD that utilize this method strongly encourage users to view their data with the area parameter. Unfortunately, even this cannot fix the problem and a dim population will expand and disappear into the noise and multiple populations with little separation on the bottom end will merge into one large, indistinguishable population.

The current version of the FACSDiVa electronics appears to use the Analog Devices AD9240AS. This converter is a 14-bit converter with a specified 78.5dB SNR capable of operation up to 10 Million Samples Per Second. Signal to Noise can be improved at lower speeds such as this 10MSPS converter, adding possibly up to one more bit in the calculations. However, trying to reduce noise by slowing the sample rate to 10MSPS or slower causes problems in high speed systems, as a 400ns pulse would only be sampled 4 times and would have very poor measurement. Thus, the pulse width of the input data must be limited to run at these speeds to achieve proper measurement, resulting in a slower machine. Some instruments, such as the BD Biosciences FACSAria®, have attempted to sidestep this by doing cuvette detection at lower velocities before going to the nozzle, but this can cause several problems in itself. First, it can add timing uncertainty which ultimately results in decreased sorting performance, limiting the sort rates possible and second, by extending the pulse width but trying to

keep high event rates, the number of hard coincidences and doublets will greatly increase.

The sample rate problem described immediately above is also influenced by the second main weakness of the Digital Processing with Single ADC architecture: DSP memory performance. Digital Signal Processors are very fast at executing instructions on the memory loaded into the registers, but time is required for the memory to get data samples into the memory, cache, and registers. At very high sample and event rates, there are tremendous amounts of data that must be processed. Using the standard frame based processing creates a memory bottleneck and limits the sample rate of the converter, which brings problems as described above.

A combination of the sample rate problems limited the current BD FACSDiVa electronics to the 10MSPS, which is believed to have played a role in the cuvette based detection design they produced, which has been shown in laboratories not to perform as well as a jet in air design.

Different methods could possibly be used to help eliminate the memory bottleneck, but the tradeoff of noise versus sample speed cannot be avoided as this is a physical limitation imposed by noise dynamics upon the converters themselves. Therefore, even with a fast enough processor, noise increases with sample rate and the problems from the first weakness are still present.

A summary of weaknesses:

- Loss of dynamic range
- Poor resolution in lower decades
- Very poor resolution in 4th decade
- Tradeoff of noise versus sample rate
- Processing bottlenecks limiting sample rate
- Potential inability to accurately process narrow pulses

Modulated Laser System

Description

In an attempt to simplify overall cytometer and electronics architecture, systems have been developed that modulate the laser sources at different frequencies and then use a single path for all lasers. Demodulation is used on the backend to separate the signals by source frequency to reduce laser crosstalk. A basic system implementing this approach is shown in Figure 4.

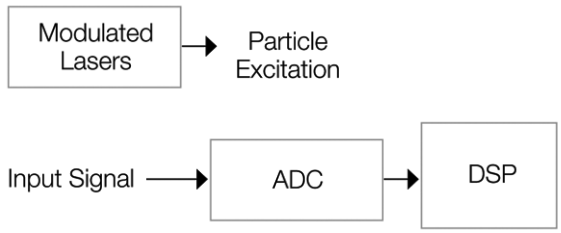

Figure 4 – Modulated Laser System Block Diagram

This architecture uses lasers modulated at different frequencies to excite particles on a single laser path, uses ADCs to convert the signal directly, and DSP processing to demodulate the signal and reconstruct the original pulse.

A variation on this system would be to use analog demodulation to reconstruct the analog signal and then any other available architecture to measure parameters from the reconstructed signal.

The iCyt Reflection® was claimed to use this method by sales representatives at ISAC 2006 (iCyt, personal communication). However, no public data was shown and no data has been made public since. Therefore, statements made about this are theoretical statements about the architecture in general.

Strengths

While very little practical information is known about a system of this type, a basic benefit is that a single laser path eliminates laser delay and allows for a collection mechanism that does not have to be based on pinholes. This could theoretically allow for higher efficiency collection of emitted light. It could also possibly simplify timing and hardware requirements.

A summary of potential strengths:

- Elimination of laser delay
- Simpler, possibly higher efficiency light collection
- Possibly simpler timing and hardware

Weaknesses

With no data available, this is again conjecture. Modulation techniques tend to work very well for communication data, where reconstruction of the original data is not necessarily bound by high resolution, high linearity and high dynamic range constraints. The input bandwidth must also be very high to allow the modulated frequencies to pass, so considerable noise can also enter the conversion stages. It is very possible that after demodulating,

the data will have distortions and lower dynamic range than other measurement architectures.

Demodulation while trying to achieve accurate pulse reconstruction also takes considerable processing, possibly limiting what can be measured.

Measurement is also based off a single ADC, so problems similar to the Digital Single ADC architecture will also affect this system.

Another problem is that not all lasers can be modulated, so laser selection is somewhat limited.

A summary of potential weaknesses:

- Pulse distortion
- Reduced dynamic range
- High processing requirements
- Poor resolution in lower decades
- Very poor resolution in 4th decade
- Tradeoff of noise versus sample rate
- Processing bottlenecks limiting sample rate
- Potential inability to process narrow pulses accuratelly
- Limited laser selection

Multi-Gain Adaptive Linear Processing (XDP)

Description

For release with the MoFlo XDP, a Multi-Gain Adaptive Linear Processing system was created to provide high resolution data with a high dynamic range while still maintaining linearity. To accomplish this, a patent pending architecture allows for digital sampling at a normal gain and a high gain and for a seamless stitching of these two stages. This yields a substantially higher dynamic range and higher resolution for small signals while still maintaining excellent linearity. A new digital architecture was also created to handle the increase in data and to provide processing rates of 100MSPS for characterizing narrow pulses. A block diagram of this system is shown in Figure 5.

This architecture uses two gain stages and high speed ADCs to bring in data from both stages simultaneously. The higher gain stage amplifies the input data by a factor of 128, providing a much bigger signal to the ADCs for small pulses. ADC data from both stages then has the offset removed with advanced digital baseline restoration and is fed to a Gain Matching and Data Stitching Unit. This module compares data from the two stages when both are valid and adjusts the gain of the two stages to stay perfectly matched. It is also responsible for merging the data from the two stages to form a seamless, high resolution output data stream with a very high dynamic range. Input data is generated from 16-bit converters and, after stitching, the output data is 23 bits. This data is then filtered to provide a 32-bit output data stream that is then used for event detection and processing.

To prevent signal offsets from being amplified by the high gain stage into very large offsets, an analog offset adjustment is added before the gain stages. Precise digital control offers the advantages of digital baseline restoration.

A new digital architecture is also utilized to allow for very high processing speeds. Input data is sampled at 100 Million Samples Per Second on both stages allowing for pulse processing of very narrow pulses. At this rate, a 400ns pulse will be sampled 40 times during the event, providing exceptional characterization. The new architecture can also process every sample of every event and can process events as fast as the backend digital bus can remove them. With the current PCI bus, 12 channels can measure, process and return at rates as fast as 600,000 events per second. Time needed between events is also as low as 30ns, allowing for direct back to back events. Digital techniques are also used for

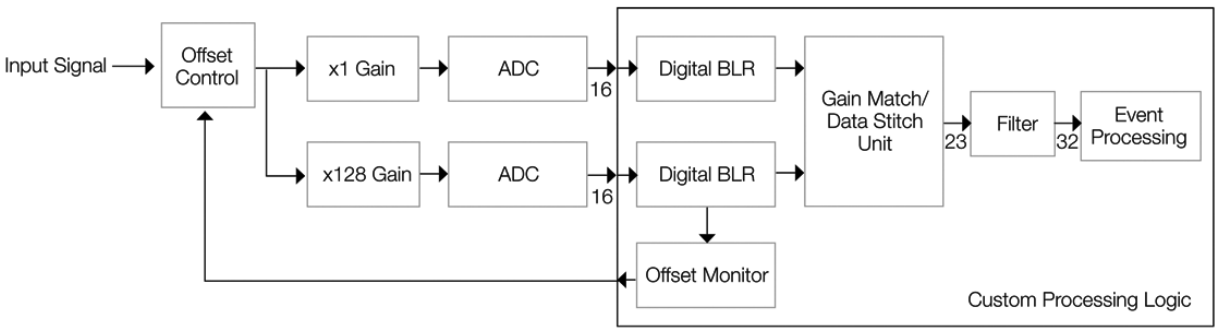

Figure 5 – Multi-Gain Adaptive Block Diagram

laser delay removal, allowing triggering from any laser without losing data.

The digital architecture is based off of Programmable System on a Chip design principles, allowing for full reprogramability of processing internals. Much more flexible than just code changes inside a DSP or standard processor, this allows for complete custom operation and full flexibility.

The MoFlo XDP will be the first cytometer to have the capabilities provided by this architecture.

Strengths

The Multi-Gain Adaptive Linear Processing architecture brings a tremendous number of benefits. First, by not having to rely on extensive analog processing, the actual hardware requirements are fairly simple. This helps reduce cost and required space, allowing for high channel densities.

By being built with PSoC design principles, the entire core processing logic can be completely changed with a simple update from software. This allows complete flexibility in event processing and virtually unlimited upgradeability.

The custom digital architecture allows for extremely high sampling rates and event rates with essentially no dead time. No other acquisition architecture on the market comes close to the processing horse-power of the XDP system. Each board has four channels and with ADCs each at 100MSPS and 16-bit data, that is over 12Gb/s of input data processing per board! For comparison, a BD board with 4 channels of 14-bit data at 10MSPS and with event rate limitations is likely less than 0.2Gb/s.

An extremely high sample rate enables unparalleled processing of narrow pulses, allowing for high speed sorting.

Digital pulse processing architecture allows for flexible and expandable extraction of event parameters.

Flexible, programmable backend allows for tremendous flexibility in event window creation and detection. Multiple detectors can be used across multiple lasers without losing any information and complex trigger equations can be used on a combination of any four channels for composite triggering. Various options are also available for event window extension, allowing for operation at zero dead time or with additional padding.

Digital BLR control with an analog front end allows for better digital control but without losing ADC range due to offsets. This provides the best possible offset removal approach in use.

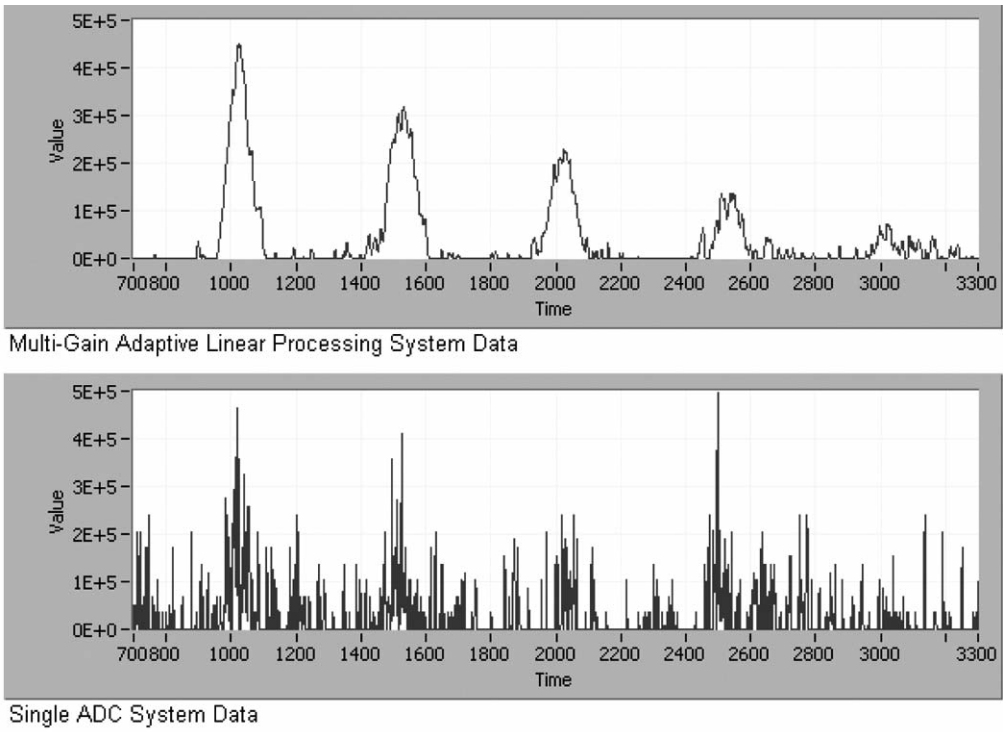

Figure 6 – System Data Comparison

The combination of gain stages and stitching techniques provides a very high dynamic range with very high resolution. For comparison, a system with only one ADC was tested along with a Multi-Gain Adaptive Linear Processing system. Each system was connected to exactly the same input source, with the input being a series of 5 pulses linearly distributed from 1mV to 100uV. Data from this test is shown in Figure 6, with graphs having the same scale.

This shows the digital sampled data (after filtering and scaling to 32-bits) for a Multi-Gain Adaptive Linear Processing System (XDP Electronics) on top and for a single ADC system on bottom. A tremendous improvement in both dynamic range and resolution can clearly be seen. In the single ADC system, the noise is higher than the 1mV pulse, which is consistent with calculations given in the weaknesses section of the single ADC digital method previously described. The XDP system, however, shows MUCH lower noise and MUCH higher resolution. Triggering on electrical noise in the lab shows the current XDP generation has peak noise just creeping into the bottom of the 5th decade. This allows for a dynamic range extending well past 4 true decades.

The patent pending technique of stitching the two gain stages together for a seamless transfer between stages has the advantage of increasing linearity between the two stages. This is done by constantly compensating for small changes in gain caused by temperature or component drift.

A summary of strengths:

- Simple hardware requirements
- Highly reprogrammable and flexible
- Extremely high sample rates
- Extremely high event rates
- Very little dead time
- Capable of processing very narrow pulses
- Digital pulse processing allows flexible parameter extraction
- Tremendous flexibility and power in triggering and event window creation
- Digital BLR with analog offset control for ideal offset adjustment
- Very high dynamic range
- High resolution
- High linearity

Feature / Benefit Summary

To provide an easy way to examine the benefits of the Multi-Gain Adaptive Linear Processing System, the strengths are summarized in Table 1.

Table 1 – Feature/Benefit Summary

Feature	Benefit
Full reprogramability/flexibility	Ability to address future needs and allow for nearly unlimited parameter extraction flexibility
Extremely high sample rate of 100MSPS	Excellent characterization of narrow pulses allow for high speed particle analysis
Extremely high event rates	Improve detection of rare events allow for higher analysis rates, allow more accurate sort decisions by not excluding any possible contaminants
Very little dead time	Allow extremely fast back to back event processing with no lost data, allow higher event rates
Digital pulse processing	Flexible extraction of event parameters, multiple parameters simultaneously, high resolution area calculation
Triggering flexibility	Ability to create composite triggers and allow a wide range of event window options, allow for higher event rates and optimized acquisition integrity
Digital BLR with analog offset control	Precise offset removal virtually immune to error at high event rates and without losing range or limiting removal range as with a normal digital BLR
High Dynamic Range	Wide range of event detection with low noise, allowing broad range data acquisition and excellent dim particle analysis
High Resolution	Provides high quality data to compensation or computed parameters for improved results without needing to dither or randomize calculation, no picket fencing in lower decades
High Linearity	Accurate results before and after compensation to provide reliable data with high integrity and repeatability

The table clearly shows the breadth and depth of the benefits provided by this new architecture.

Weaknesses

This architecture is not yet known to contain any significant weaknesses. Properly designing the analog gain stages to track each other correctly during pulses and without adding much noise is somewhat tricky but can and has been accomplished. Also, creating a full, custom PSoC backend takes more time than using traditional DSP technology, but again this can and has been done. Any weaknesses found in the field with the architecture can also most likely be taken care of with updated logic, as the system is fully reprogrammable.

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